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EXAMINER	
SHERMAN, STEPHEN G	
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2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/661,535	HIRAKAWA ET AL.	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *8 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed the 20 June 2007. Claims 1-6 and 8-22 are pending. Claim 7 has been cancelled.

Response to Arguments

2. Applicant's arguments with respect to claim 1-6 and 8-21 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-5 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Correa et al. (EP 1,174,850 A1) in view of Sano et al. (US 6,115,011).

Regarding claim 1, Correa et al. disclose a method for driving a plasma display panel, wherein a display field comprises a plurality of successive subfields having at least two different luminance rations, producing a gradation display, each display subfield comprises at least an address period to write cells to be lit in the display subfield in accordance with corresponding display data and a sustain period to cause light emission to occur in the written cells (Paragraph [0021]), said method comprising:

writing, after generating an all-write discharge, in the address period of a selected one of the plurality of successive display subfields in each display field, all of the cells to be written in the respective address periods of the plurality of successive display subfields in the display field, including the selected subfield (Paragraph [0012] and Paragraph [0022] explain that a priming pulse causes a discharge where all-cells are illuminated. Paragraphs [0025]-[0029] explain that the first subfield is used to write all of the cells that are not to be black, i.e. all cells to be written in the display field. The chart at the top of column 6 illustrates this point, since there is a 0 in the first subfield for display data "0" and a 1 in the first subfield for all other display data levels.), and

applying sustain pulses to cause light emission in the respective sustain periods of the successive display subfields of the display field (Paragraph [0021] explains that subfields contain a sustain period to cause light emission.).

Correa et al. fail to teach of generating successively two or more all-cell write discharges in the priming period.

Sano et al. disclose a method for driving a plasma display panel, comprising generating successively two or more all-cell write discharges in the priming period (Figure 7 and column 2, lines 21-34 and column 6, lines 11-29 and 35-42 explain that multiple discharges can be caused to occur in the priming period.).

Therefore, it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to provide for multiple discharges as taught by Sano et al. in the priming period taught by Correa et al. in order to use the priming discharging in an advantageous way so as to control the brightness of the entire image on the screen.

Regarding claim 2, Correa et al. and Sano et al. disclose the method for driving a plasma display panel, as set forth in claim 1.

Correa et al. also disclose wherein a first subfield in the display field is has the lowest luminance ration, and a second subfield has the second lowest luminance ratio (Paragraphs [0027]-[0028].).

Regarding claim 3, Correa et al. and Sano et al. disclose the method for driving a plasma display panel, as set forth in claim 1.

Correa et al. also disclose wherein a display field has a display subfield with a same luminance ratio as that of the selected display subfield, in addition to selected display subfield (Paragraph [0027] explains that there are 2 subfields with the weight of "1.").

Regarding claim 4, Correa et al. and Sano et al. disclose the method for driving a plasma display panel, as set forth in claim 1.

Correa et al. also disclose wherein the selected display subfield is the display subfield at the head in a display field (Paragraphs [0027]-[0028].).

Regarding claim 5, Correa et al. and Sano et al. disclose the method for driving a plasma display panel, as set forth in claim 1.

Correa et al. also disclose wherein the all-cell write discharges are caused to occur in the selected display subfield before the address period (Figure 2, soft-priming occurs before the address period.).

Regarding claim 19, Correa et al. and Sano et al. disclose the method for driving a plasma display panel, as set forth in claim 1.

Correa et al. also disclose wherein the gradation display level is determined with the luminance due to lighting in the predetermined subfield being taken into consideration (The chart on the top of column 6 shows that the luminance takes into account the first subfield.).

Regarding claim 20, please refer to the rejection of claim 1, and furthermore Correa et al. also disclose a plasma display device comprising a plasma display panel and a driving circuit for the plasma display panel (Figure 4).

Regarding claim 21, this claim is rejected under the same rationale as claims 1 and 2.

Regarding claim 22, this claim is rejected under the same rationale as claims 1 and 4.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 6 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Correa et al. (EP 1,174,850 A1) in view of Sano et al. (US 6,115,011) and further in view of Awaji (JP 2000-148085 A).

Regarding claim 6, Correa et al. and Sano et al. disclose a method for driving a plasma display panel, as set forth in claim 1.

Correa et al. also disclose wherein an all-cell write discharge is caused to occur in the selected display subfield before the address period (Figure 2, soft-priming occurs before the address period.).

Correa et al. and Sano et al. fail to teach wherein the selected display subfield is also a subfield with a heavy weight of luminance.

Awaji discloses of an all-cell write discharge that occurs in a subfield with a heavy weight of luminance (Paragraph [0017]. The examiner interprets that the largest subfield is the one with the heavy weight of luminance.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the method of having an all-cell write discharge that occurs in a subfield with a heavy weight of luminance as taught by Awaji with the method of driving a plasma display panel as taught by the combination of Correa et al. and Sano et al. in order to provide a plasma display panel drive method that produces a stable discharge effect while increasing contrast.

Regarding claim 9, Correa et al. and Sano et al. disclose the method for driving a plasma display panel, as set forth in claim 1.

Correa et al. also disclose wherein the display subfield with the lowest luminance ratio is arranged at the head in a display field (Paragraph [0027].).

Correa et al. and Sano et al. fail to teach wherein the selected display subfield is arranged in the second position in the display field.

Awaji discloses wherein the selected display subfield is arranged in the second position in the display field (Drawing 3 and paragraphs [0029]-[0032]. The examiner interprets that since the discharge occurs in sf2, that this is the subfield in the second position and that the display field at the head is the one with the lowest luminance ratio since the sustain period for that subfield is the smallest.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the method of having the selected display subfield is arranged in the second position in the display field as taught by Awaji with the method of driving a plasma display panel as taught by the combination Correa et al. and Sano et al. in order to provide a plasma display panel drive method that produces a stable discharge effect while increasing contrast.

Regarding claim 10, Correa et al., Sano et al. and Awaji disclose the method for driving a plasma display panel, as set forth in claim 9.

Awaji also discloses wherein the selected display subfield is one with the second lowest luminance ratio (Drawing 3 and paragraph [0031]. The examiner interprets that since sf2 is in the second position and has the second smallest sustain period that it is the subfield with the second lowest luminance ratio.).

Regarding claim 11, Correa et al., Sano et al. and Awaji disclose the method for driving a plasma display panel, as set forth in claim 9.

Correa et al. also disclose wherein an all-cell write discharge is caused to occur in the subfield at the head and the selected display subfield before the address period (Figure 2 shows that soft-priming occurs before the address period in the head subfield.).

9. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Correa et al. (EP 1,174,850 A1) in view of Sano et al. (US 6,115,011) and further in view of Tokunaga et al. (US 2003/0067425).

Regarding claim 8, Correa et al. and Sano et al. disclose the method for driving a plasma display panel, as set forth in claim 5.

Correa et al. and Sano et al. fail to teach a method wherein a display subfield reset discharge is caused to occur in order to erase the residual charges in a lit cell in the display subfield immediately before the display subfield in which the all-cell write discharge is caused to occur.

Tokunaga et al. disclose a method for driving a plasma display panel wherein a display subfield reset discharge is caused to occur in order to erase the residual charges in a lit cell in the display subfield immediately before another display subfield (Figure 18 and paragraph [0158]. The examiner interprets that the erasure stage E is a stage in which a reset discharge is caused to occur in order to erase the residual charges in a lit cell, and that since this occurs in every cell the erasure stage would occur before the predetermined subfield.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the method of having a reset discharge in a subfield as taught by Tokunaga et al. with the method taught by the combination of Correa et al. and Sano et al. in order to provide a display device and a method of driving a display panel which are capable of improving the dark contrast.

10. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Correa et al. (EP 1,174,850 A1) in view of Sano et al. (US 6,115,011) and further in view of Awaji (JP 2000-148085 A) and Tokunaga et al. (US 2003/0067425).

Regarding claim 12, Correa et al., Sano et al. and Awaji disclose the method for driving a plasma display panel, as set forth in claim 9.

Correa et al., and Sano et al. and Awaji fail to disclose a method wherein a display subfield reset discharge is caused to occur in order to erase the residual charges in a lit cell in the display subfield at the head.

Tokunaga et al. disclose a method for driving a plasma display panel wherein a display subfield reset discharge is caused to occur in order to erase the residual charges in a lit cell in the display subfield at the head (Figure 18 and paragraph [0158]. The examiner interprets that the erasure stage E is a stage in which a reset discharge is caused to occur in order to erase the residual charges in a lit cell, and the E stage is shown to be in the subfield at the head.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the method of having a reset discharge in a subfield at the head as taught by Tokunaga et al. with the method taught by the combination of Correa et al., Sano et al. and Awaji in order to provide a display device and a method of driving a display panel which are capable of improving the dark contrast.

11. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Correa et al. (EP 1,174,850 A1) in view of Sano et al. (US 6,115,011) and further in view of Moon (US 2003/0098826).

Regarding claim 13, Correa et al. and Sano et al. disclose the method for driving a plasma display panel, as set forth in claim 1.

Correa et al. and Sano et al. fail to teach of the method wherein the widths of an address pulse and a scan pulse during the address period in the selected display subfield are wider than those of the address pulse and the scan pulse during the address period in other display subfields.

Moon discloses a method for driving a plasma display panel wherein the widths of an address pulse and a scan pulse during the address period in a display subfield are wider than those of the address pulse and the scan pulse during the address period in other display subfields (Paragraphs [0069]-[0071]. The examiner interprets that since the width of the scan pulses of some scan lines are larger than others and that the data pulses synchronized with the scan pulses are also set to be larger that the scan and address pulse applied during an address period would be wider than those in other subfields.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the method of having wider pulses in the predetermined subfield as taught by Moon with the method taught by the combination of Correa et al. and Sano et al. in order to allow for the cells to generate high luminance.

12. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Correa et al. (EP 1,174,850 A1) in view of Sano et al. (US 6,115,011) and further view of Hashimoto et al. (US 2001/0017605) and Tokunaga et al. (JP 2000-276106 A).

Regarding claim 14, Correa et al. and Sano et al. disclose the method for driving a plasma display panel, as set forth in claim 1.

Correa et al. and Sano et al. fail to teach a method wherein the voltage of an address pulse during the address period in a subfield is raised.

Hashimoto et al. disclose a method for driving a plasma display panel wherein the voltage of an address pulse during the address period in a subfield is raised (Paragraph [0070].).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the method of raising the voltage of an address pulse as taught by Hashimoto et al. with the method taught by the combination of Correa et al. and Sano et al. in order to increase writing probability.

Correa et al., Sano et al. and Hashimoto et al. fail to teach a method for driving a plasma display panel wherein the voltage of a pulse in a subfield in larger than the voltage of pulses in the other subfields.

Tokunaga et al. disclose a method for driving a plasma display panel wherein the voltage of a pulse in a subfield in larger than the voltage of pulses in the other subfields (Abstract: Solution. The examiner interprets that since one subfield is indicated as to having a pulse with a larger voltage than the other subfields, that this subfield could be the predetermined subfield.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the method of having a larger pulse voltage in the predetermined subfield as taught by Tokunaga et al. with the method taught by the combination of Correa et al., Sano et al. and Hashimoto et al. in order to enhance contrast with low power consumption while suppressing a spurious profile also and moreover to enhance display quality by stabilizing selective discharge.

13. Claims 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Correa et al. (EP 1,174,850 A1) in view of Sano et al. (US 6,115,011) and further in view of Tokunaga et al. (JP 2000-276106 A).

Regarding claim 15, Correa et al. and Sano et al. disclose the method for driving a plasma display panel, as set forth in claim 1.

Correa et al. and Sano et al. fail to teach a method wherein the voltage of a scan pulse during the address period in the selected display subfield is greater than that of the scan pulse during the address period in other display subfields.

Tokunaga et al. disclose a method for driving a plasma display panel wherein the voltage of a scan pulse during the address period in a selected display subfield is greater than that of the scan pulse during the address period in other display subfields (Abstract: Solution. The examiner interprets that since one subfield is indicated as to having a scanning pulse with a larger voltage than the other subfields, that this subfield could be the predetermined subfield.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the method of having a larger scanning voltage in the predetermined subfield as taught by Tokunaga et al. with the method taught by the combination of Correa et al. and Sano et al. in order to enhance contrast with low power consumption while suppressing a spurious profile also and moreover to enhance display quality by stabilizing selective discharge.

14. Claims 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Correa et al. (EP 1,174,850 A1) in view of Sano et al. (US 6,115,011) and further in view of Kanazawa et al. (US 2001/0054993).

Regarding claim 16, Correa et al. and Sano et al. disclose the method for driving a plasma display panel, as set forth in claim 1.

Correa et al. and Sano et al. fail to teach a method for driving a plasma display panel wherein a process to suppress a discharge in an unlit cell is performed between the address period and the sustain period in the selected display subfield.

Kanazawa et al. disclose a method for driving a plasma display panel wherein a process to suppress a discharge in an unlit cell is performed between the address period and the sustain period in a selected display subfield (Figure 17 and paragraphs [0083]-[0084]. The examiner interprets that the voltage applied to generate an auxiliary discharge is a process to suppress a discharge in an unlit cell.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the method of adding an additional pulse period as taught by Kanazawa et al. with the method for driving a plasma display panel as taught by the combination of Correa et al. and Sano et al. in order to extinguish a wall charge of a cell in which an erroneous discharge has occurred.

Regarding claim 17, Correa et al., Sano et al. and Kanazawa et al. disclose the method for driving a plasma display panel, as set forth in claim 16.

Kanazawa et al. also disclose wherein the process to suppress a discharge in an unlit cell is a process in which, at the same time an address pulse is applied to an address electrode (Figure 17, P1 is a pulse applied to the address electrode.), a pulse, the applied voltage of which varies as time elapses, is applied to a scan electrode (Figure 17. The pulse applied during the additional pulse period on X(X2) starts at 0V the reduces to –50V, therefore the voltage applied during the period varies as time elapses.).

Regarding claim 18, Correa et al., Sano et al. and Kanazawa et al. disclose the method for driving a plasma display panel, as set forth in claim 17.

Kanazawa et al. also disclose wherein the final potential of the pulse, the applied voltage of which varies as time elapses (Figure 17, the final potential of the pulse is -50V), is lower than the finally reached potential of a charge control pulse, the applied voltage of which varies as time elapses (Figure 17, the examiner interprets that the pulse applied to the address electrode, which starts at 0V and raises to 50 V, is the charge control pulse, in which the –50V pulse is lower than the 50V pulse.).

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

16 June 2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER